REMARKS

Claims 24-33 and 44-45 have been canceled without prejudice. New claims 46-55 have been added. Claims 46-55 are pending. Reexamination and allowance of the pending claims is respectfully requested.

Claims 24-27, 32-33 and 44 stand rejected under 35 U.S.C. 103(a) as being unpatentable over USP 6,375,062 to Higdon et al. ("Higdon") in view of USP 6,392,143 to Kosjio ("Koshio"). 28-31 and 45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Higdon in view of Koshio, and further in view of one or more other secondary references. These rejections are respectfully traversed with respect to the new claims.

Claims 24-33 and 44-45 have been canceled without prejudice and replaced by new claims 46-56, of which claim 46 is the only pending independent claim. Independent claim 46 recites a method of forming electroplated solder on an organic circuit board for attaching an IC chip using the steps outlined in the claim. In the Office Action, the Examiner asserts that Higdon discloses that "the substrate/circuit board may be a flexible circuit", and this premise forms the basis for the rejection. In other words, the Examiner asserts that the fact that Higdon mentioned a "flexible circuit" in column 1, lines 23-25 means that Higdon's method can be applied to flexible circuits. However, Applicant respectfully submits that Higdon does ***not*** teach or suggest that its method can be applied to form electroplated solder on a flexible or organic circuit board for attaching an IC chip. ***This is the critical issue which determines the merits of the rejection: does Higdon teach that its method can be used to form electroplated solder on organic circuit boards ("the Issue")?***

Applicant wishes to thank the Examiner for his courtesy in granting the undersigned a personal interview on December 6, 2005. During the interview, the undersigned and the Examiner discussed the merits of the Issue. To begin with, the preamble in new claim 46 recites "a method of forming electroplated solder on an organic circuit board for attaching an IC chip". In contrast, Higdon teaches the method of forming electroplated solder on the IC chip, but it does not teach the method of

forming electroplated solder on an organic circuit board.

In addition, the undersigned pointed out that there are significant differences between forming electroplated solder on an organic circuit board and forming electroplated solder on an IC chip (which is disclosed in connection with Higdon's method) which make it impossible to apply the technology and methods for manufacturing an IC chip onto manufacturing organic circuit boards. The undersigned and the Examiner re-read pages 4-6 of Applicant's Appeal Brief dated May 27, 2005 ("the Appeal Brief") which outline the reasons why Higdon's method cannot be applied to form electroplated solder on an organic circuit board. In summary:

1. application of the high temperatures and acid/alkali environments used for forming electroplated solder on the IC chip will destroy the organic circuit board; and

2. the chemical solutions used for processing the IC chip will attack the organic circuit board.

The undersigned argued at the interview that a person skilled in the art would readily recognize that the techniques and processes used for forming electroplated solder on IC chips cannot be applied to form electroplated solder on organic circuit boards.

The Examiner and the undersigned discussed the implication of Higdon's mention of a flexible circuit in column 1 (i.e., the Issue). As set forth above, the Examiner believes that this mere mention of a flexible circuit means that Higdon's method can be applied to flexible circuits. In contrast, Applicant believes that this mention of a flexible circuit is in connection with a discussion of the prior art, and there is no teaching or suggestion in Higdon which states that the method described in the Detailed Description section of Higdon can be applied to form electroplated solder on an organic circuit board for attaching an IC chip. The Federal Circuit has made it clear that each prior art reference must be read in its entirety, and within the proper context. Thus, when a person skilled in the art reads Higdon, this person will interpret the mention of a flexible circuit as being in the context of the prior art, and this person will understand that the method disclosed in Higdon cannot be applied to form electroplated

solder on an organic circuit board for attaching an IC chip.

To further highlight this distinction, new claim 46 includes the following limitations which are not disclosed in Higdon:

> "forming a first thin ***non-noble*** metal layer that is deposited by electroless plating over the board surface;
>
> forming a second thin metal layer that is deposited by electroplating over the first thin metal film;
>
> .....
>
> reflowing the solder material to form a solder bump, wherein the first and second thin metal layers beneath the solder bump are dissolved completely into the solder bump."

Support for these limitations can be found on page 9, line 26 to page 10, line 10 of the specification. By forming a first thin metal layer (which is ***not noble metal***) that is deposited by electroless plating over the board surface, and then forming a second thin metal layer that is deposited by electroplating over the first thin metal film, the claimed invention mitigates the damage to the solder mask layer, "... since the catalytic copper (which is not noble metal) can be easily removed in said etching solution". See page 10, lines 5-7 of the specification.

During the interview, the Examiner asserted that these steps are well-known in the art, and are disclosed in column 5, lines 5-9 and 42-49 of Higdon. Applicant respectfully submits that column 5, lines 5-9 and 42-49 of Higdon do not expressly teach or suggest the provision of multiple metal layers deposited by electroless plating, and dissolving these two layers into the solder bump. Higdon fails to expressly disclose these steps because Higdon is not concerned with the issues relating to forming electroplated solder on a flexible or organic circuit board for attaching an IC chip.

In light of these reasons, it is respectfully submitted that all pending claims are in condition for allowance. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any amendments, ideas or suggestions for placing this application in condition for allowance.

Respectfully Submitted,

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Dated: December 16, 2005

CERTIFICATE OF MAILING

I hereby certify that this paper and its enclosures are being deposited with the United States Postal service as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Date: December 16, 2005 By: _____
Raymond Sun